

STUDY MODULE DESCRIPTION FORM		
Name of the module/subject Microprocessors systems		Code 1010331141010332704
Field of study Control Engineering and Robotics	Profile of study (general academic, practical) (brak)	Year /Semester 2 / 4
Elective path/specialty -	Subject offered in: polish	Course (compulsory, elective) obligatory
Cycle of study: First-cycle studies	Form of study (full-time, part-time) full-time	
No. of hours Lecture: 2 Classes: - Laboratory: 2 Project/seminars: -		No. of credits 5
Status of the course in the study program (Basic, major, other) (brak)		(university-wide, from another field) (brak)
Education areas and fields of science and art technical sciences		ECTS distribution (number and %) 5 100%
Responsible for subject / lecturer: dr inż. Krzysztof Chmiel email: krzysztof.chmiel@put.poznan.pl tel. 61 665 35 31 Wydział Elektryczny ul. Piotrowo 3A 60-965 Poznań		
Prerequisites in terms of knowledge, skills and social competencies:		
1	Knowledge	K_W00: K_W01:
2	Skills	K_U01: K_U06:
3	Social competencies	K_K00: K_K04:
Assumptions and objectives of the course: Knowledge of mathematical models, methods of synthesis and CAD tools of digital circuits.		
Study outcomes and reference to the educational results for a field of study		
Knowledge:		
1. [K_W03] - [-]		
Skills:		
1. [K_U03] - [-]		
2. [K-U08] - [-]		
Social competencies:		
1. [K_K04] - [-]		
2. [K_K07] - [-]		
Assessment methods of study outcomes		
Credit for lectures and laboratory exercises.		
Course description		

Combinatorial and sequential digital circuits. Boolean functions and finite automata as mathematical models of the circuits. Realization of Boolean functions with use of logic gates, multiplexors, demultiplexors, ROMs and logic arrays. Realization of automata with use of flip-flops. Integrated digital circuits. Microprogrammed circuits and flow diagrams. Concurrent circuits and Petri nets. CAD tools.

Laboratory program:

1. Analysis of combinatorial circuits (UK)
2. Synthesis of combinatorial circuits
3. Realization of UK with use of NAND gates
4. Realization of UK with use of multiplexors
5. Realization of UK with use of demultiplexors
6. Realization of UK with use of ROMs
7. Analysis of sequential circuits (US)
8. Realization of US with use of D-NAND structure
9. Realization of US with use of JK-NAND structure
10. Realization of US with use of memory-register structure
11. Realization of asynchronous US
12. Realization of microprogrammed circuits ? control circuit
13. Realization of microprogrammed circuits ? operational circuit
14. Realization of concurrent circuits
15. Conclusion

Basic bibliography:

1. Teoria układów logicznych, K. Chmiel, Wydawnictwo Politechniki Poznańskiej, Poznań, 1994, 1995
2. Układy cyfrowe - wykłady, K. Chmiel, PowerPoint, Poznań, 2004

Additional bibliography:

1. Układy scalone TTL w systemach cyfrowych, J. Pierńkos, J. Turczyński, WNT, Warszawa, 1980
2. Podstawy projektowania układów cyfrowych, C. Zieliński, PWN, Warszawa, 2003

Result of average student's workload

Activity	Time (working hours)
1. Lectures.	30
2. Laboratory exercises.	30
3. Consultations and examination.	15
4. Preparation to laboratory exercises and elaboration of reports.	30
5. Preparation to tests and examination.	20

Student's workload

Source of workload	hours	ECTS
Total workload	125	5
Contact hours	65	2
Practical activities	60	2